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| APPLICATION NO. | FILING DATE | FIRST NAMED INVENTOR | ATTORNEY DOCKET NO. | CONFIRMATION NO. |
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| 10/808,288 | 03/25/2004 | Christophe Maleville | 4717-10500 | 5090 |

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| EXAMINER | |
|---|---|
| ISAAC, STANETTA D | |

| ART UNIT | PAPER NUMBER |
|---|---|
| 2812 | |

DATE MAILED: 12/15/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

| Office Action Summary | Application No. | Applicant(s) | |
|---|---|---|---|
| | 10/808,288 | MALEVILLE ET AL. | |
| | Examiner | Art Unit | |
| | Stanetta D. Isaac | 2812 | |

*-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --*

**Period for Reply**

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

**Status**

1)☒ Responsive to communication(s) filed on *06 September 2005*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

**Disposition of Claims**

4)☒ Claim(s) *1-18* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-18* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

**Application Papers**

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *25 March 2004* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

**Priority under 35 U.S.C. § 119**

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Lynne A. Gurley

**LYNNE A. GURLEY**
**PRIMARY PATENT EXAMINER**
**TC 2800, AU 2812**

**Attachment(s)**

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

## DETAILED ACTION

This Office Action is in response to the amendment filed on 9/06/05. Currently, claims 1-18 are pending.

### *Specification*

The specification has not been checked to the extent necessary to determine the presence of all possible minor errors. Applicant's cooperation is requested in correcting any errors of which applicant may become aware in the specification.

### *Claim Rejections - 35 USC § 103*

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 1-4 and 6-18 are rejected under 35 U.S.C. 103(a) as being unpatentable over Yokokawa et al., US Patent 6,312,797 in view of Toshima et al., Patent Application Publication US 2002/0155709.

Yokokawa discloses the semiconductor method substantially as claimed. See figure 1, and corresponding text, where Yokokawa shows, pertaining to claim 1, a method for preparing a bonding surface of a semiconductor layer of a wafer comprising: treating the bonding surface to oxidize contaminants (figure 1; col. 4, lines 30-67; col. 5, lines 1-6; col. 6, lines 19-35); cleaning the bonding surface to remove essentially all remaining contaminants (figure 1; col. 4, lines 54-

67; col. 5, lines 1-6; col. 6, lines 19-35); and then oxidizing the bonding surface (figure 1; col. 4, lines 35-44, ***Note***: the Examiner takes the position that the silicon oxide film, as taught by Yokokawa, includes an silicon oxide layer formed by oxidation). In addition, Yokokawa shows, pertaining to claim 2, wherein the cleaning of the bonding surface comprises treating the bonding surface with a first solution capable of removing isolated and encrusted particles, and then treating the bonding surface with a second solution capable of removing metallic contamination (col. 4, lines 54-67; col. 5, lines 1-6). Also, Yokokawa shows, pertaining to claim 3, wherein the first solution is a SC1 solution that includes ammonium hydroxide ($NH_4OH$), hydrogen peroxide ($H_2O_2$) and deionized water (col. 4, lines 54-67; col. 6, lines 19-35). Yokokawa shows, pertaining to claim 4, wherein the second solution SC2 solution that includes hydrochloric acid (HCl), hydrogen peroxide ($H_2O_2$) and deionized water (col. 4, lines 54-67; col. 6, lines 19-35). In addition, Yokokawa shows, pertaining to claim 7, which further comprises preparing a bonding surface of a second wafer by treating the bonding surface to oxidize contaminants (col. 4, lines 30-67; col. 5, lines 1-6), cleaning the bonding surface to remove essentially all remaining contaminants (figure 1; col. 4, lines 54-67; col. 5, lines 1-6; col. 6, lines 19-35), followed by contacting the bonding surface of the first wafer to the bonding surface of the second wafer to effect bonding therebetween and form a structure (figure 1; col. 5, lines 20-45). Also, Yokokawa shows, pertaining to claim 9, further comprises applying a heat treatment to the structure to strengthen the bond between the first and second wafers (col. 5, lines 45-57). Yokokawa shows, pertaining to claim 10, wherein the bonding surface of the second wafer exists on an oxide layer (figure 1; col. 5, lines 26-45). In addition, Yokokawa shows, pertaining to claim 11, wherein the semiconductor structure is a semiconductor on insulator (SOI) structure (figure 1; col. 5, lines

58-67; col. 6, lines 1-3). Also, Yokokawa shows, pertaining to claim 12, wherein the oxide layer is an insulating layer (col. 5, lines 26-45). Yokokawa shows, pertaining to claim 13, wherein the bonding surfaces of each of the first and second wafers exist on an oxide layer (figure 1; col. 5, lines 20-26). In addition, Yokokawa shows, pertaining to claim 14, wherein each oxide layer is an insulating layer (figure 1; col. 5, lines 20-26). Also, Yokokawa shows, pertaining to claim 15, wherein at least one of the first or second wafers includes a zone of weakness to facilitate detachment of the structure (figure 1; col. 4, lines 45-54; col. 5, lines 27-45). Yokokawa shows, pertaining to claim 16, wherein the semiconductor wafer comprises silicon, germanium, SiGe, AlGaAs, GaAS, InGaAs, AlGaAsP, InGaAsP, InP, or another Group III-Group V semiconductor or Group II-Group VI semiconductor (col. 4, lines 30-34). Finally, Yokokawa shows, pertaining to claim 17, wherein the first wafer includes a zone of weakness to facilitate detachment of a layer that includes the bonding surface (figure 1; col. 4, lines 45-54; col. 5, 27-45).

Yokokawa shows, pertaining to claim 18, in a method for preparing a bonding surface of a semiconductor layer of a wafer for bonding to a second wafer wherein the bonding surface is cleaned to remove contaminants (figure 1; col. 4, lines 54-67; col. 5, lines 1-6; col. 5, lines 20-26),

However, Yokokawa fails to show, pertaining to claims 1, 7 and 18, and the oxidizing the bonding surface with ozone to improve the hydrophilic properties of the bonding surface. In addition, Yokokawa fails to show shows, pertaining to claim 6, wherein the oxidizing comprises at least one of immersing the bonding surface in an ozone bath, or spraying ozone droplets onto the bonding surface, or exposing the bonding surface to an ozone gas. Finally, Yokokawa fails

to show, pertaining to claim 8, wherein the bonding is at least partly achieved by hydrophilic adhesion of the bonding surfaces of the first and second wafers.

Toshima teaches, in figures 1-14, and corresponding text where it is conventionally known that a surface of a semiconductor wafer can by made to have hydrophilic properties by treating the wafer with an ozone solution to form an oxidation film on the surface of the semiconductor wafer (paragraphs [0006], [0009-0010], [0013-0014]).

It would have been obvious to one of ordinary skill in the art, to substitute the following steps of: oxidizing the bonding surface with ozone to improve the hydrophilic properties of the bonding surface; wherein the oxidizing comprises at least one of immersing the bonding surface in an ozone bath, or spraying ozone droplets onto the bonding surface, or exposing the bonding surface to an ozone gas; wherein the bonding is at least partly achieved by hydrophilic adhesion of the bonding surfaces of the first and second wafers, in the method of Yokokawa, pertaining to claims 1, 6-8 and 18, according to the teachings of Toshima, with the motivation that, by forming the oxide insulating film with an ozone solution, the advantage would be to improve the hydrophilic properties of the surface of the semiconductor wafer, resulting in a more efficient bonding surface technique for the two wafers. In addition, since both Yokokawa and Toshima teaches the formation of an oxide layer, forming an oxide insulating film by an ozone solution would prove to be equivalent since ultimately an oxide layer will be formed on the surface of the semiconductor wafer.

Claim 5 is rejected under 35 U.S.C. 103(a) as being unpatentable over Yokokawa et al., US Patent 6,312,797 in view of *Stanley Wolf and Richard N. Tauber, Silicon Processing For The VLSI Era, 2000, Lattice Press, Second Edition, pages 135-137.*

Yokokawa discloses the semiconductor method substantially as claimed. See preceding rejection of claims 1-4 and 6-18 under 35 U.S.C. 102(b).

However, Yokokawa fails to show pertaining to claim 5, wherein the cleaning step includes applying ultrasonic energy to assist in removing particulate contamination from the bonding surface.

Wolf teaches, on pages 135-137, a conventional method of removing particles from wafers that involves the use of ultrasonic energy.

It would have been obvious to one of ordinary skill in the art to incorporate, wherein the cleaning step includes applying ultrasonic energy to assist in removing particulate contamination from the bonding surface, in the method of Yokokawa, pertaining to claim 5, according to the conventional teachings of Wolf, with the motivation that by using a cleaning technique that includes the use of ultrasonic energy, the removal of the contaminates can be performed without any physical contact to the wafer making the contamination removal more effective.

### ***Response to Arguments***

Applicant's arguments with respect to claims 1-18 have been considered but are moot in view of the new ground(s) of rejection.

***Conclusion***

Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Stanetta D. Isaac whose telephone number is 571-272-1671. The examiner can normally be reached on Monday-Friday 9:30am -6:30pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Michael Lebentritt can be reached on 571-272-1873. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Stanetta Isaac
Patent Examiner
December 7, 2005

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